REMARKS

Upon entry of the instant amendment, claims 1 and 4-19 are pending. Claims 2 and 3 have been cancelled. Claims 1, 4, 5, 8-10, and 13 have been amended. Claims 16-19 have been added. Claim 13 was found to define patentable subject matter but was objected to for depending on rejected claims. Claim 13 was thus converted to an independent claim and was amended to include all of the limitations of the rejected base claim and intervening claims. Claim 13 was also amended to overcome the claim objections set forth on page 2 of the Detailed Action. Accordingly, claim 13 should be allowable. Claims 14 and 15 depend on claim 13. Claims 14 and 15 should also be allowable. Claims 16-19 have been added. These claims are dependent claims and recite subject matter clearly supported by the specification. In particular, the subject matter set forth in claim 16 can be found in paragraph [0053] on page 10. The subject matter of claim 17 is found in paragraph [0087] and in particular in Table 6. The support for claims 18 and 19 is found throughout the specification. Claim 1 has been amended to define patentable subject matter over the references of record. Claims 1, 9-10 and 13 have also been amended to overcome the objections set forth on page 2 of the Detailed Action. Claim 4 has been amended to recite the subject matter set forth in paragraph [0039] of the specification. It is respectfully submitted that the application is in condition for allowance.

Before getting into the specific rejections, two other matters need to be addressed. First, future correspondence regarding this case is to be addressed to the undersigned. Secondly, the Examiner is respectfully requested to make all admitted prior art being relied on to support the rejection under 35 U.S.C. §103 of record.

CLAIM OBJECTIONS:

Claims 1, 5, 9, 10 and 13 have been objected to for various reasons as set forth on page 2 of the Detailed Action. It is respectfully submitted that each and every one of these claims has been amended as suggested on page 2 of the Detailed Action. Accordingly, these objections should all be overcome.

CLAIM REJECTIONS - 35 U.S.C. §102:

Claims 1-4 have been rejected under 35 U.S.C. §102(b) as being anticipated by "A Technique for Modeling S-Parameters for HEMT Structures as a Function of Gate Bias", by *Mahon et al.,* IEEE Transactions on Microwave Theory and Techniques, Vol. 40, No. 7, July 1992 ("*Mahon et al.*"). Claims 2 and 3 have been cancelled. Thus, the rejection in regard to claims 2 and 3 is obviated. With respect to claims 1 and 4, in order for there to be anticipation, each and every one of the elements of the claims must be found in a single reference. It is respectfully submitted that the claims recite subject matter not disclosed or suggested by the *Mahon et al.* reference. For example, claims 1 and 4 recite that the electrical circuit elements are derived from a small signal analysis of at least one of the intrinsic charge and electric charge within the semiconductor device.

The *Mahon et al.* reference discloses a model for predicting the device S-parameters as a function of gate bias. Even though the *Mahon et al.* reference discloses a physically based model, it does not disclose or suggest that the model is derived from an analysis of the intrinsic charge and/or electric field within the semiconductor. Thus, it is respectfully submitted that the *Mahon et al.* patent does not anticipate nor suggest the invention recited in claims 1 and 4. For these reasons, the Examiner is respectfully requested to reconsider and withdraw this rejection.

CLAIM REJECTIONS - 35 U.S.C. §103:

Claims 5-7 have been rejected under 35 U.S.C. §103 as being unpatentable over the *Mahon et al.* reference in view of the admitted prior art. Claims 5-7 are dependent upon claim 1. As such, these claims recite that the physical model is based at least in part based upon the intrinsic charge and/or electrical field characteristics of the semiconductor device. As mentioned above, the *Mahon et al.* reference does not disclose or suggest a physical model based on such characteristics. Likewise, the admitted prior art does not disclose or suggest a model based on these characteristics. For these reasons and the above reasons, it is respectfully submitted that claims 5-7 recite patentable subject matter over the *Mahon et al.* reference and the admitted prior art. The Examiner is thus respectfully requested to reconsider and withdraw the rejection of claims 5-7.

Claims 8-12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the *Mahon et al.* patent in view of the admitted prior art and further in view of: "A Possible Scaling Limit for Enhancement-Mode GaAs MESFET's in DCFL Circuits", by *Hirose et al.*, IEEE Transactions on Electron Devices, Vol. 39, No. 12, Dec. 1992 (*"Hirose et al."*). Claims 8-12 are further dependent on claim 1. As discussed above, these claims recite, in combination, a method for modeling a semiconductor device, based at least in part on the intrinsic charge and electric field characteristics within the semiconductor device. As discussed above, such a method is not disclosed or suggested in either the *Mahon et al.* or admitted prior art. Likewise, such a method is also not disclosed in the *Hirose et al.* reference. For these reasons and all of the above reasons, the Examiner is respectfully requested to reconsider and withdraw the rejections of claims 8-12.

CONCLUSION

An earnest attempt has been made to address all of the issues in the Official Action. An early allowance is thus earnestly solicited.

Respectfully submitted,

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ATTACHMENT FOR CLAIM AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/840,600; Filed April 23, 2001

1. (Amended) A method of modeling a semiconductor device comprising the steps of:

a) modeling a small signal electrical equivalent circuit for said [semi conductor] semiconductor device which includes a plurality of electrical circuit elements defining a small signal model, said small signal equivalent circuit based in part on one or more real process parameters;

b) deriving said electrical circuit elements at least in part from a small signal excitation analysis of at least one [or more predetermined] of the intrinsic charge and electrical field characteristics of said semiconductor device.

4. (Amended) The method as recited in claim 1, wherein [step (b) further includes deriving the electrical circuit element from a small signal excitation analysis of the electric fields within the device] said real process parameters include at least one of: gate length recess, etch depth, recess undercut dimensions and passivation nitrite thickness.

5. (Amended) The method as recited in claim [2]1, wherein step (b) includes the [following] step of:

[d)]determining the relationships between one or more [the] conduction band offsets and electrical permitivities and the material composition for the materials in the semiconductor device.

8. (Amended) The method as recited in claim 5, further including step (e); determining the electron transport characteristics of any bulk materials in the semiconductor device.

9. (Amended) The method as recited in claim 8, further including step (f); determining [the] an undepleted linear channel mobility.

10. (Amended) The method as recited in claim 9, wherein step [(b)] (f) is determined by material characterization.

13. (Amended) [The] A method [as recited in claim 12, further including step (h)] of modeling a semiconductor device comprising the steps of:

(a) modeling a small signal on an electrical equivalent circuit for said semiconductor device with a plurality of electrical circuit elements defining a small signal model;

deriving said electrical circuit elements from a small signal excitation analysis of the intrinsic charge within said semiconductor device by determining the relationships between one or more of the conduction band offsets and electrical permitivities and the material composition for the materials in the semiconductor device;

determining the electron transport characteristics of any bulk materials in the semiconductor device;

determining an undepleted linear channel mobility;

forming [semi-physical] semiconductor physical equations with empirical terms for modeling one or more of the following characteristics: fundamental-charge control physics for

sheet charge in [the] an active channel as controlled by [the] a gate terminal voltage; average centroid position of the sheet charge within the active channel width; position of charge partitioning boundaries as a function of gate, drain and source terminal voltages; bias dependence of linear channel mobility and surface depleted regions; bias dependence of [the] a velocity saturating electric field of the channel; saturated electron velocity; electrical conductance within the linear region of the channel, under the gate; electrical conductance within the source and drain access regions.

16. The method as recited in claim 1, wherein said semiconductor device model is based at least in part as a function of one or more of: conduction band offsets; electrical permitivities; and material composition of the epi stack.

17. The method as recited in claim 4, wherein said real process parameters further include: gate-source recess, gate-drain recess, gate-source spacing and source-drain spacing.

18. The method as recited in claim 1, wherein said semiconductor device is a high electron mobility transistor (HEMT).

19. The method as recited in claim 1, wherein said semiconductor device is a field effect transistor (FET).